

**What is Claimed is:**

1. A method of selective plating on a circuit substrate comprising:  
applying a first metal pattern to a surface of the substrate;  
applying a second metal pattern to the surface of the substrate, the  
5 second metal pattern being electrically isolated from the first metal pattern;  
creating a potential voltage difference between the first metal pattern  
and a metal source comprising a metal of a first type, wherein the voltage  
potential of the first metal pattern is less than the voltage potential of the metal  
source; and  
10 plating the first metal pattern with the metal of a first type, the plating  
the first metal pattern comprising attracting the metal of a first type to the  
voltage potential of the first metal pattern.
2. The selective plating method of claim 1,  
wherein creating a potential voltage difference comprises applying a  
15 negative charge to the first metal pattern; and  
wherein plating the first metal pattern comprises attracting the metal of  
a first type to the negative charge applied to the first metal pattern.
3. The selective plating method of claim 1, wherein creating a  
potential voltage difference comprises:  
20 applying a positive charge to the metal source; and  
electrically coupling the first metal pattern to ground.
4. The selective plating method of claim 1 further comprising:

creating a potential voltage difference between the second metal pattern and a metal source comprising a metal of a second type, wherein the voltage potential of the second metal pattern is less than the voltage potential of the first metal pattern; and

5           plating the second metal pattern with the metal of a second type, the plating the second metal pattern comprising attracting the metal of a second type to the voltage potential of the second metal pattern.

5.       The selective plating method of claim 1 further comprising:  
electrically coupling the first metal pattern to a cathode;  
10       electrically coupling the second metal pattern to an anode; and  
electrically coupling the anode to the metal source.

6.       The selective plating method of claim 1 further comprising  
creating a potential voltage difference between the first metal pattern and the second metal pattern, wherein the voltage potential of the first metal pattern is  
15       less than the voltage potential of the second metal pattern.

7.       The selective plating method of claim 1 further comprising  
electrically coupling the first metal pattern to a first via in the substrate,  
wherein creating a potential voltage difference comprises one of  
applying a negative charge to the first metal pattern through the first via or  
20       electrically coupling the first metal pattern to ground through the first via.

8.       The selective plating method of claim 7 further comprising:

electrically coupling the second metal pattern to a second via in the substrate;

applying a positive charge to the second metal pattern through the second via; and

5           creating a potential voltage difference between the first metal pattern and the second metal pattern, wherein the voltage potential of the first metal pattern is less than the voltage potential of the second metal pattern.

9.       The selective plating method of claim 1 further comprising:  
positioning a heat sink in an opening in the substrate; and  
10       brazing the heat sink to the substrate around the opening to provide a hermetic seal.

10.      A circuit package comprising:  
a base portion having a first surface, a second surface, a first via, a second via, and a plurality of pins;  
15       a first metal pattern disposed on the first surface;  
a second metal pattern disposed on the second surface, the second metal pattern being electrically coupled to the first via; and  
a third metal pattern disposed on the second surface and arranged to form a gap to electrically isolate the second metal pattern from the third metal  
20       pattern, the third metal pattern being electrically coupled to the first metal pattern through the second via.

11.      The circuit package of claim 10, wherein the base portion comprises a substrate.

12. The circuit package of claim 10, wherein the base portion  
comprises a ceramic substrate.

13. The circuit package of claim 10, wherein the base portion  
comprises one of an alumina substrate and an aluminum nitride (AlN)  
5 substrate.

14. The circuit package of claim 10 further comprising a nickel-  
plated pattern electrolytically disposed on the second metal pattern.

15. The circuit package of claim 10 further comprising a gold-  
plated pattern electrolytically disposed on the third metal pattern.

10 16. The circuit package of claim 10 further comprising a single  
heat sink arranged to dissipate heat from a device built on the circuit package,  
wherein the base portion comprises an opening arranged to engage the  
heat sink, and

wherein the third metal pattern comprises an opening arranged to  
15 expose the device to the heat sink.

17. The circuit package of claim 16,  
wherein the base portion opening comprises a first perimeter edge, and  
wherein the heat sink comprises:

a body having the same size and same shape as the base portion  
20 opening, and

a flange extending outwardly from the body having a second  
perimeter edge larger than the first perimeter edge.

18. The circuit package of claim 16, wherein the heat sink is engaged with the base portion via a braze alloy, the braze alloy providing a hermetic seal between the opening and the heat sink.

19. The circuit package of claim 18, wherein the braze alloy  
5 comprises a copper silver braze alloy.

20. The circuit package of claim 16, wherein the heat sink comprises a copper tungsten alloy heat sink.

21. The circuit package of claim 16,  
wherein the heat sink comprises an upper surface and a lower surface  
10 having more surface area than the upper surface, and  
wherein the upper surface is exposed on the second base portion surface and the lower surface is exposed on the first base portion surface when the heat sink is engaged with the base portion.

22. A circuit package comprising:  
15 a substrate having a plurality of pins, a top surface, a bottom surface, a first via, a second via and an opening; and  
a single heat sink having a top surface and a bottom surface, the heat sink positioned within the opening such that the top surface is exposed through the top surface of the substrate and the bottom surface is exposed through the  
20 bottom surface of the substrate.

23. The circuit package of claim 22 further comprising:

a first metal pattern disposed on the top surface and electrically  
coupled to the first via;

a second metal pattern disposed on the bottom surface and electrically  
coupled to the second via, the second metal pattern being electrically isolated  
5 from the first metal pattern.

24. The circuit package of claim 23 further comprising:

a first plated pattern electrolytically disposed on the first metal pattern;  
and

a second plated pattern electrolytically disposed on the second metal  
10 pattern.

25. The circuit package of claim 24, wherein the first plated pattern  
comprises a gold plated pattern.

26. The circuit package of claim 24, wherein the second plated  
pattern comprises a nickel plated pattern.

15 27. The circuit package of claim 22,  
wherein the opening comprises a first perimeter edge, and  
wherein the heat sink comprises:

a body having the same size and same shape as the opening,  
and

20 a flange extending outwardly from the body having a second  
perimeter edge larger than the first perimeter edge.

28. The circuit package of claim 22, wherein the heat sink is engaged with the base portion via a braze alloy, the braze alloy providing a hermetic seal between the opening and the heat sink.

29. The circuit package of claim 28, wherein the braze alloy  
5 comprises a copper silver braze alloy.

30. The circuit package of claim 22, wherein the heat sink comprises a copper tungsten alloy heat sink.